

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2002-319006

(43)Date of publication of application : 31.10.2002

(51)Int.Cl.

G06K 19/00
B42D 15/10
D21H 21/42
D21H 27/30
G06K 19/07
// G07D 7/10

(21)Application number : 2001-121104

(71)Applicant : TOKUSHU PAPER MFG CO LTD
HITACHI LTD

(22)Date of filing : 19.04.2001

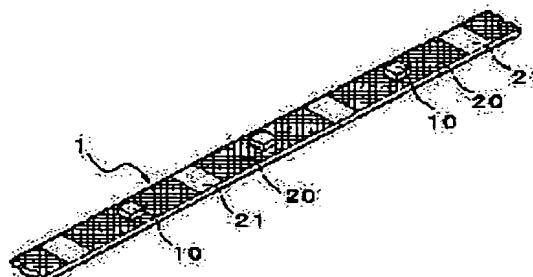
(72)Inventor : MURAKAMI TORU
AKAHORI SHINICHI
AKIYAMA KOSUKE
USAMI MITSUO

(54) ANTI-COUNTERFEIT THREAD, ANTI-COUNTERFEIT SHEET-SHAPED MATERIAL USING IT, AND METHOD OF MANUFACTURING IT

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a technique for inserting fine semiconductor chips into a sheet- shaped material such as a paper sheet or a plastic sheet in order to further enhance the anti-counterfeit effect of conventional anti-counterfeit paper with threads therein, capable of easily and efficiently inserting even refined semiconductor chips into the sheet-shaped material.

SOLUTION: A strip 1 having affixed thereto semiconductor chips 10 each having a built-in memory with a plurality of bits and antenna wiring and each 0.5 mm or less long on one side is either affixed to the surface of the sheet-shaped material or inserted into the sheet-shaped material to obtain the anti-counterfeit sheet-shaped material. The semiconductor chip enables information to be written and read by noncontact method, ensuring a determination as to whether the sheet- shaped material is true or false by reading information recorded in the semiconductor chips contained in the sheet-shaped material. The thread is given timing marks 21 each serving as an indication of the affixed position of the semiconductor chip, so that by inserting the thread into the sheet-shaped material while detecting the marks, the semiconductor chips can be accurately and efficiently inserted into predetermined positions on the sheet-shaped material.



LEGAL STATUS

[Date of request for examination] 27.12.2004

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

* NOTICES *

JPO and NCIP are not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3. In the drawings, any words are not translated.

CLAIMS

[Claim(s)]

[Claim 1] The thread for forged prevention characterized by having pasted one side of the film which carried out the slit of the one-side semiconductor chip 0.5mm or less which contained two or more bits memory, and was equipped with antenna wiring to narrow-width.

[Claim 2] The thread for forged prevention according to claim 1 characterized by giving the timing mark used as the rule of thumb of the adhesion location of said semiconductor chip to said thread.

[Claim 3] The sheet-like object for forged prevention characterized by pasting the thread of claims 1 or 2 together on the front face of a sheet-like object, or having inserted in the interior of a sheet-like object.

[Claim 4] The sheet-like object for forged prevention according to claim 3 characterized by said sheet-like object being paper or a plastic sheet.

[Claim 5] The manufacture approach of the sheet-like object for forged prevention which is the approach of pasting the thread of claim 2 together on the front face of paper or a plastic sheet, and manufacturing the sheet-like object for forged prevention, and is characterized by to paste a thread together so that said semiconductor chip may be located in a predetermined location by adjusting the tension of the thread at the time of pasting, detecting the location of the timing mark formed in paper or a plastic sheet, and the timing mark given to the thread.

[Claim 6] The manufacture approach of the sheet-like object for forged prevention according to claim 5 characterized by forming the slot for pasting a thread together in the front face of said paper or a plastic sheet.

[Claim 7] It is the approach of manufacturing the multilayer sheet-like object for forged prevention which consists of pasting two or more sheets of papers, or plastic sheets together, inserting the thread of claim 2 between two or more sheets of papers, or plastic sheets. By adjusting the tension of the thread at the time of insertion, detecting the location of the timing mark formed in paper or a plastic sheet, and the timing mark given to the thread. The manufacture approach of the sheet-like object for forged prevention characterized by inserting a thread so that said semiconductor chip may be located in a predetermined location.

[Claim 8] The manufacture approach of the sheet-like object for forged prevention according to claim 7 characterized by forming the slot for inserting a thread in the front face of at least one sheet of said paper or a plastic sheet.

[Claim 9] The forged prevention form characterized by being ***** as the thread of claims 1 or 2 is buried in paper.

[Claim 10] The forged prevention form according to claim 9 characterized by the aperture aperture section which made thickness of paper thin intermittently being formed, and making it expose a thread in this aperture aperture section.

[Claim 11] The forged prevention form characterized by having inserted the thread of claims 1 or 2 between the paper of the **** doubling paper which consists of two-layer at least.

[Claim 12] The forged prevention form according to claim 11 characterized by the aperture aperture section being formed intermittently of two-layer to one layer at least, and making it expose a thread in this aperture aperture section.

[Claim 13] It is the manufacture approach of the forged prevention form which consists of things. ***** of the paper of an outermost layer of drum, and the paper of a inner layer which consists of two-layer at least — a multi-tub type cylinder machine — using — manufacturing — facing — between paper — the thread of claim 2 — inserting — ***** — said semiconductor chip is located in a predetermined location by adjusting the tension of the thread at the time of insertion, detecting the location of the timing mark formed in paper, and the

timing mark given to the thread -- as -- a thread -- inserting -- ***** -- the manufacture approach of the forged prevention form characterized by things.

[Translation done.]